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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,538	08/25/2003	Mark S. Isenberger	042390P17323	4672
7590	04/28/2005			
			EXAMINER	
			NGUYEN, DAO H	
			ART UNIT	PAPER NUMBER
			2818	
DATE MAILED: 04/28/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

EX

Office Action Summary	Application No.	Applicant(s)	
	10/648,538	ISENBERGER, MARK S.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 04/07/2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-10 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 24 August 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>0305</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In response to the communications dated 08/25/2003 through 04/07/2005, claims 1-10 are active in this application.

Claim(s) 11-15 have not been elected without traverse and have been cancelled.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 03/25/2005. The references cited on the PTOL 1449 form have been considered.

Specification

3. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-10 are provisionally rejected under 35 U.S.C. 103(a) as being obvious over copending Application No. 2004/0214351 by Agarwal et al., which has a common subject with the instant application, in view of U.S. Patent No. 5,691,551 to Eimori.

Based upon the earlier effective U.S. filing date of the copending application, it would constitute prior art under 35 U.S.C. 102(e) if published or patented. This provisional rejection under 35 U.S.C. 103(a) is based upon a presumption of future publication or patenting of the conflicting application.

This provisional rejection might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the copending application was derived from the inventor of this application and is thus not the invention "by another," or by a showing of a date of invention for the instant application prior to the effective U.S. filing date of the copending application under 37 CFR 1.131. This rejection might also be overcome by showing that the copending application is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 1, Agarwal discloses a polymer memory, as shown in figs. 1-6, comprising:

a first plurality of conductive word lines 14/16/18 extending parallel to one another in a y-direction and having center lines spaced from one another by a first distance in an x-direction;

a first ferroelectric polymer memory material 30 in x- and y-directions over the word lines;

a plurality of conductive bit lines 32/34/36 extending parallel to one another in the x-direction over the first ferroelectric polymer memory material 30 and having center lines spaced from one another by a second distance in the y-direction, a first array of polymer memory cells being defined in the first ferroelectric polymer memory material, each where a respective bit line crosses over a respective one of the first plurality of word lines, such that the ferroelectric polymer memory material at a respective cell of the first array is changed when a select voltage difference is applied over respective word and bit lines on opposing sides of the respective cell (see paragraph [0003]).

Agarwal is silent about the distance(s) between the central lines of the word lines and the distance(s) between the central lines of the bit lines.

Eimori discloses a memory device comprising memory cell or storage node 17 between word lines 4 and bit lines 15, wherein the distance(s) between the central lines

of the bit lines 15 being larger than the distance(s) between the central lines of the word lines 4 (see figs. 1, 4-6).

Therefore, It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Agarwal so that it would have the distance(s) between the central lines of the bit lines (or of the word lines; notice: the terms "word lines" and "bit lines" in the pending application are interchangeable (specification, page 5, lines 1-6)) being less than that of the word lines (or bit lines) in order to obtain a memory cell structure of high production yield and high reliability (see the abstract, and col. 3, lines 29-36).

Regarding claim 2, Agarwal disclose the polymer memory further comprising:
a second ferroelectric polymer memory material in x- and y-directions over the bit lines; and a second plurality of conductive word lines extending parallel to one another in the y-direction over the second ferroelectric polymer memory material and having center lines spaced from one another by a third distance, equal to the first distance, in the x-direction, a second array of polymer memory cells being defined in the second ferroelectric polymer memory material, each where a respective one of the second plurality of word lines crosses over a respective bit line, such that the ferroelectric polymer memory material at a respective cell of the respective second array is changed when a select voltage difference is applied over respective bit and

word lines opposing the respective cell. See figs. 7. It is further noticed that though the memory structure of Agarwal is a multilevel memory array wherein a substrate and a second level of word lines are interposed between the first level of bit lines and the second ferroelectric polymer memory material, it would have been well known in the art that such memory structure can be modified to have the second ferroelectric polymer memory material disposing directly on the first level of bit lines and sharing the first level of bit lines with the first ferroelectric polymer memory material (see also U.S. Patent No. 6,034,882 to Johnson et al. for further details).

Regarding claim 3, Agarwal/Eimori discloses the polymer memory comprising all claimed limitations. See col. 6, line 8 to col. 7, line 61.

Regarding claim 4, Agarwal/Eimori discloses the polymer memory wherein adjacent ones of the word lines are spaced from one another by a first spacing in the x-direction, and adjacent ones of the bit lines are spaced from one another by a second spacing in the y-direction, the first spacing being more than the second spacing. See figs. 1, 4-6.

Regarding claim 5, Agarwal discloses a polymer memory, as shown in figs. 1, 4-6, comprising:

a plurality of multi-layer constructions 60/60', each including a plurality of bit lines 34/36/38 extending parallel to one another in an x-direction and having center lines

spaced from one another by a first distance in a y-direction, ferroelectric polymer memory material 30 on first and second opposing sides of the bit lines 34/36/38, and first and second pluralities of conductive word lines 14/16/18 with the ferroelectric polymer memory material 30 and bit lines 34/36/38 between the first and second pluralities of word lines 14/16/18, the word lines of each plurality extending parallel to one another in the y-direction and having center lines spaced from one another by a second distance in the x-direction,

a plurality of insulating layers 12, each between a respective pair of the multi-layer constructions.

Agarwal is silent about the distance(s) between the central lines of the word lines and the distance(s) between the central lines of the bit lines.

Eimori discloses a memory device comprising memory cell or storage node 17 between word lines 4 and bit lines 15, wherein the distance(s) between the central lines of the bit lines 15 being larger than the distance(s) between the central lines of the word lines 4 (see figs. 1, 4-6).

Therefore, It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Agarwal so that it would have the distance(s) between the central lines of the bit lines (or of the word lines; notice: the terms "word lines" and "bit lines" in the pending application are

interchangeable (specification, page 5, lines 1-6)) being less than that of the word lines (or bit lines) in order to obtain a memory cell structure of high production yield and high reliability (see the abstract, and col. 3, lines 29-36). It is further noticed that though the memory structure of Agarwal is a multilevel memory array wherein a substrate and a second level of word lines are interposed between the first level of bit lines and the second ferroelectric polymer memory material, it would have been well known in the art that such memory structure can be modified to have the second ferroelectric polymer memory material and a second word lines disposing directly on the first level of bit lines and sharing the first level of bit lines with the first ferroelectric polymer memory material and the first word lines (see also U.S. Patent No. 6,034,882 to Johnson et al., col. 5, line 30 to col. 11, line 38 for further details).

Regarding claim 6, Agarwal/Eimori disclose the polymer memory wherein each word line has a first width in the x-direction and each bit line has a second width in the y-direction, the second width being less than the first width. See col. 6, line 8 to col. 7, line 61.

Regarding claim 7, Agarwal/Eimori discloses the polymer memory where adjacent ones of the word lines are spaced from one another by a first spacing in the x-direction and adjacent ones of the bit lines are spaced from one another by a second spacing in the y-direction, the first spacing being more than the second spacing. See figs. 1, 4-6 of Eimori.

Regarding claim 8, Agarwal discloses a polymer memory, as shown in figs. 1-6, comprising alternating layers of conductive lines (14/16/18)/(34/36/38) and ferroelectric polymer memory material 30, some of the layers of conductive lines having word lines (14/16/18) extending in a y-direction and other ones of the layers of conductive lines having bit lines (34/36/38) extending in an x-direction, the conductive lines of some of the layers (word lines) having center lines spaced by a first distance and conductive lines of other ones (bit lines) of the layers having center lines spaced by a second distance.

Agarwal is silent about the distance(s) between the central lines of the word lines and the distance(s) between the central lines of the bit lines.

Eimori discloses a memory device comprising memory cell or storage node 17 between word lines 4 and bit lines 15, wherein the distance(s) between the central lines of the bit lines 15 being larger than the distance(s) between the central lines of the word lines 4 (see figs. 1, 4-6).

Therefore, It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Agarwal so that it would have the distance(s) between the central lines of the bit lines (or of the word lines; notice: the terms "word lines" and "bit lines" in the pending application are

interchangeable (specification, page 5, lines 1-6)) being less than that of the word lines (or bit lines) in order to obtain a memory cell structure of high production yield and high reliability (see the abstract, and col. 3, lines 29-36).

Regarding claims 9-10, these limitations are inherent because the layers of bit lines are shared layers, so they must be less than the layers of word lines.

Conclusion

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.



Dao H. Nguyen
Art Unit 2818
April 25, 2005



David Neims
Supervisory Patent Examiner
Technology Center 2800